On-chip Context Save and Restore (CSR) and Hardware Task Relocation (HTR)

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CHREC NSF Center for High-Performance Reconfigurable Computing

Aurelio Morales
Dr. Ann Gordon-Ross

UF UNIVERSITY of FLORIDA

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Introduction

Goals

- Develop ***system services*** to enhance partial reconfiguration (PR) in high-performance embedded reconfigurable computing (RC) systems
  - Gives users control over application development
  - Releases the user to deal with complex processes done on FPGAs
  - Maximizes distributed computing between networked/pooled FPGA resources

Motivations

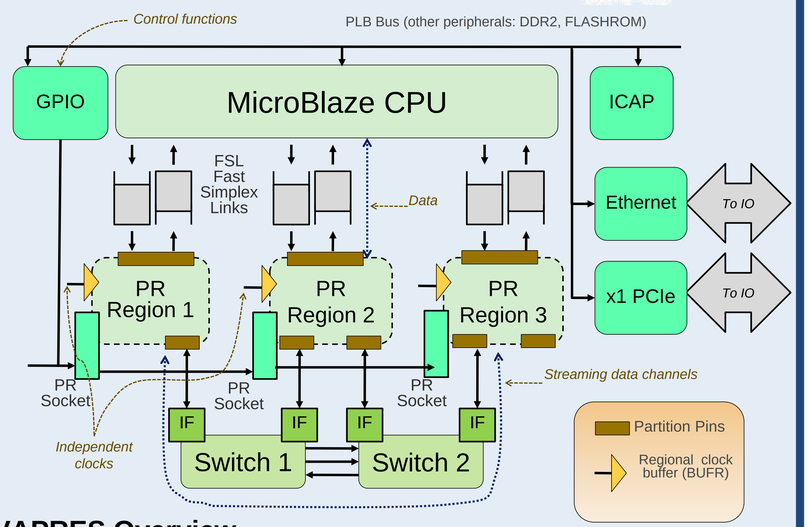
- PR enables area and power savings
- PR-capable FPGAs enable preemption/resumption of PR modules (PRMs)/tasks in PRRs without losing PRM's execution state
- Cost-effective, scalable, and flexible base architecture (VAPRES) facilitates distributed computing system development and management

Approach

- Leverage network of PR-capable FPGAs (e.g., VAPRES FPGAs) for increased (distributed) resource pool
- Distributed system services efficiently manage networked resources
  - Context save and restore (CSR), hardware task relocation (HTR), and distributed dynamic resource manager (DDRM)

Accomplished Tasks

- New functionalities for on-chip CSR and HTR
  - Support for LUTRAM, BRAM, and DSP resources in PRRs
  - Support for multiple rows and columns in PRRs
  - Reduced execution times for CSR and HTR



VAPRES Overview

- Multi-purpose, flexible, and scalable PR base architecture
- Simplifies use of and communication between PRRs and PRMs
- DDRM efficiently manages VAPRES resources and task execution
  - DDRM leverages CSR to prevent loss of PRM execution state
  - DDRM leverages HTR to maximize PRM/PRR throughput/utilization

VAPRES – Virtual Architecture for Partially Reconfigurable Embedded Systems
PRM – Partially Reconfigurable Module
PRR – Partially Reconfigurable Region

CLB – Configurable Logic Block
ICAP – Internal Configuration Access Port
GPIO – General Purpose Input/Output

On-chip Context Save and Restore (CSR)

Overview

- CSR provides a mechanism to capture execution state of preempted PRMs and resume execution in the same PRR

Approach

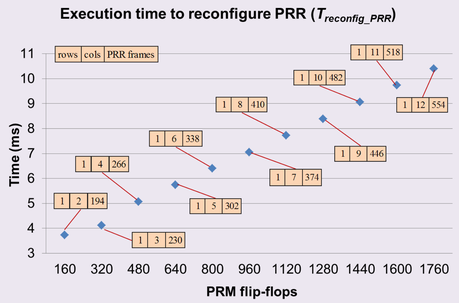
- Software approach for portability purposes across different FPGAs
- Context save (CS) and context restore (CR) via ICAP
  - CS: Checkpoint PRM's current execution state (i.e., context)
  - CR: Restore checkpointed PRM execution state
- Implement as a C program on MicroBlaze

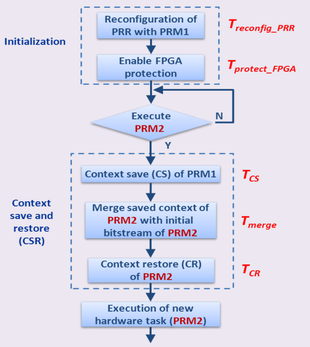
Benefits

- On-chip, no external device required
- Enhances hardware multitasking over shared PRRs
- Avoids lengthy PRM re-execution time on resumption
- No tool flow changes needed
- Portable accross any application and system
- Enables system designers to trade off CSR times and PRM/PRR sizes

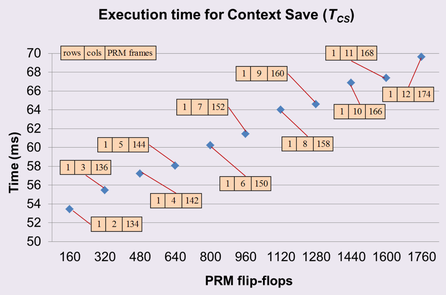
Experiments

- VAPRES static region: MicroBlaze, UART, Ethernet interface, FSLs, ICAP, GPIOs, DDR2 SDRAM, Compact Flash interface
- PRRs: Each PRR implements two or more PRMs
- Testbed: Virtex5 LX110T, 100 MHz, 1 PRR, ML509, Linux OS



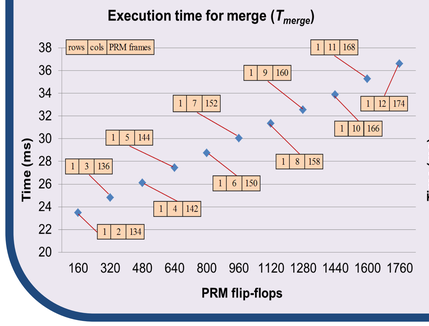


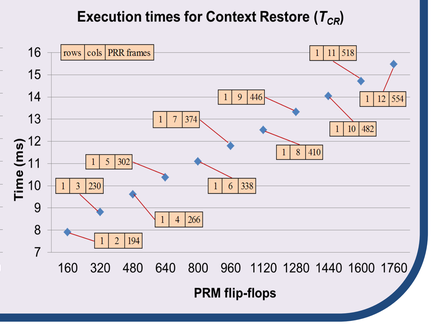
Context save and restore flow (1 PRR, 2 PRMs)



CSR flow details

- Example: 1 PRR, 2 PRMs
  - PRR: CLBs, one BRAM column
  - PRR is 1 row, many columns
- Protection
  - Entire FPGA before operations
  - Only on PRR after CS/CR
- Unprotection
  - Only on PRR before CS/CR





On-chip Hardware Task Relocation (HTR)

Overview

- HTR provides a mechanism to relocate previously saved PRM context to any free PRR with enough resources

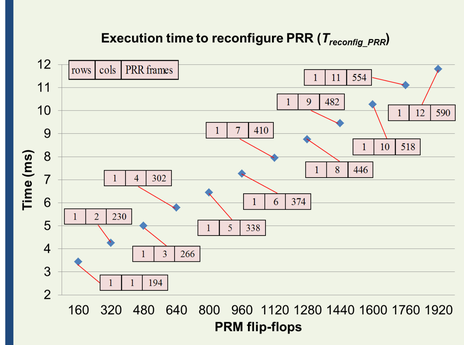
Approach

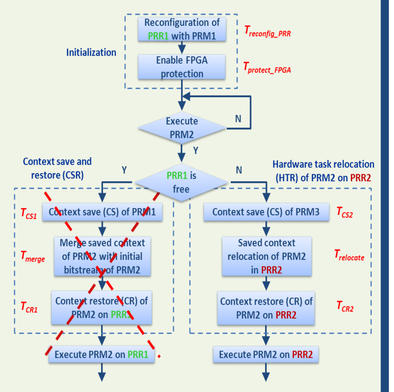
- Leverage CSR functionality
  - Relocates saved context using CS on one PRR and CR to a different PRR
  - Generates relocated partial bitstream from initial-state partial bitstream and saved-context partial bitstream
- HTR between heterogeneous PRRs
  - PRRs with different sizes/resources/positions on device
  - No special constraints on PRRs or static region

Benefits in Addition to CSR

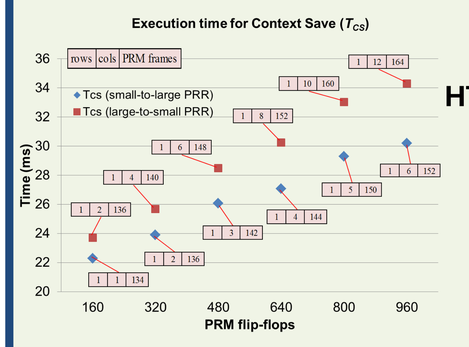
- Preemption and resumption of PRMs in different PRRs
- Improves PRM scheduling performance and task throughput
- Maximizes shared resource utilization, reduces idle PRRs

Testbed: Virtex5 LX110T, 100 MHz, 2 PRRs, ML509





Hardware task relocation flow (2 PRRs, PRM2 in both PRRs)



HTR flow details

- Example: 2 PRR, 2 PRMs/PRR
  - PRM2 for both PRRs
  - PRRs: CLBs, one BRAM column
- Relocation
  - Only during context restore
  - Primary PRR is not available for PRM2
- Protection/Unprotection
  - Same as CSR